

CLMPTO 09/28/04 JW

Cancel Claims 91-98, 136-148, 154

99. (Previously Amended): A method for automatically constructing a routing tag for a cell based on an address provided by a bus operation on a bus connected to a first node of a system interconnect comprising the steps of:

- capturing said address from said bus;
- converting said address into a value stored in said routing tag;
- detecting an interrupt condition change at said first node, said interrupt condition change comprising either an interrupt assertion or an interrupt deassertion;
- creating an interrupt cell at said first node responsive to the detecting said interrupt condition change, said interrupt cell addressed to a second node and containing said interrupt condition change;
- transporting said interrupt cell to said second node; and
- asserting an interrupt signal at said second node responsive to said interrupt condition change.

100. (Previously Presented): The method of claim 99 wherein the step of asserting further comprises steps of:

- recombining said interrupt cell containing said interrupt assertion at said second node; and
- transmitting an updown signal.

101. (Previously Presented): The method of claim 100 wherein the step of asserting further comprises steps of:

- detecting that said updown signal is non-zero; and
- asserting an interrupt at said second node.

102. (Previously Presented): The method of claim 99 wherein said cell further comprises a first node identifier and the step of asserting further comprises:

- storing said first node identifier and said interrupt condition change.

103. (Previously Presented): The method of claim 99 wherein the step of asserting further comprises steps of:

- recombining said interrupt cell containing said interrupt deassertion; and
- transmitting an updown signal.

104. (Previously Presented): The method of claim 101 wherein the step of asserting further comprises steps of:

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clearing said said up/down counter to zero; and
clearing an interrupt at said second node.

106. (Previously Presented): The method of claim 99 wherein said interrupt will occur when an interrupt occurs on the bus and the step of asserting further comprises asserting said interrupt condition with a second node (interrupt) locally with.

107. (Previously Presented): The method of claim 99 wherein said interrupt condition is a result of a bus error on said bus.

108. (Previously Presented): The method of claim 106 wherein said bus is a PCI bus and said bus error condition is a BUSERR condition.

Claims 109-121 (Continued).

109. (Previously Presented): A method for substantially converting a pending bus cell based on an address provided by a bus operation on a bus connected to a first node of a system, the method comprising the steps of:

- extracting said address from said bus;
- converting said address into a value stored in said memory; and
- converting said bus operation into said cell;

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transferring said cell over said system interconnect from said first node to a second node;
and
performing an equivalent bus operation on a second computer system bus by said second node after receipt of said cell by said second node.

110. (Previously Presented): The method of claim 109 wherein said first bus is a PCI bus and said second bus is a second PCI bus.

111. (Previously Presented): The method of claim 110 wherein said first bus is a PCI bus and said second bus is not.

112. (Previously Presented): The method of claim 111 further comprising steps of:
asserting a second cell containing status of said equivalent bus operation;
transferring said second cell to said first node;
completing said bus operation upon receipt of said second cell.

113. (Previously Presented): The method of claim 112 wherein the step of converting includes steps of:

- determining, responsive to said bus operation, an identifier for said second node bus operation;
- mapping constant addressable memory (CAM); and
- including said identifier in said cell.

127. (Previously Presented): An apparatus for substantially constructing a routing tag for a cell based on an address provided by a bus operation on a bus connected to a first node of a system in accordance comprising:

an address capturing mechanism configured to capture said address from said bus;

an address conversion mechanism configured to convert said address from said bus into a value stored in said routing tag of said cell;

an interrupt detection mechanism configured to detect an interrupt condition change at said first node, said interrupt condition change comprising either an interrupt assertion or an interrupt deassertion;

an interrupt cell assertion mechanism configured to assert an interrupt cell at said first node responsive to the interrupt detection mechanism, said interrupt cell being addressed to a second node and containing said interrupt condition change;

a cell transportation mechanism configured to transport said interrupt cell to said second node;

an interrupt assertion mechanism configured to assert an interrupt signal at said second node responsive to said interrupt condition change.

128. (Previously Presented): The apparatus of claim 127 wherein the interrupt assertion mechanism further comprises:

an interrupt assertion condition mechanism at said second node configured to recognize said interrupt cell containing said interrupt assertion and transport an up/down counter;

129. (Previously Presented): The apparatus of claim 128 wherein the interrupt assertion mechanism further comprises:

a port interrupt mechanism configured to detect that said up/down counter is non-zero and to port an interrupt at said second node.

130. (Previously Presented): The apparatus of claim 127 or claim 128 further comprising a first node identifier and the interrupt assertion mechanism further comprises:

a storage mechanism configured to store said first node identifier and said interrupt condition change.

131. (Previously Presented): The apparatus of claim 127 wherein the interrupt assertion mechanism further comprises:

an interrupt deassertion condition mechanism at said second node configured to recognize said interrupt cell containing said interrupt deassertion and transport an up/down counter.

132. (Previously Presented): The apparatus of claim 110 wherein the interrupt assertion mechanism further comprises:

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a clear interrupt mechanism configured to detect that said upstream source is gone and to clear an interrupt at said second node.

133. (Previously Presented): The apparatus of claim 132 wherein said interrupt cell comprises an interrupt security code and the interrupt instruction mechanism further comprises:

an interrupt security mechanism configured to match said interrupt security code with a second node interrupt security code.

134. (Previously Presented): The apparatus of claim 132 wherein said interrupt condition is a result of a bus error on said bus.

135. (Previously Presented): The apparatus of claim 134 wherein said bus is a PCI bus and said bus error results in a BUSERR assertion.

Claims 136-140 (Canceled).

141. (Previously Amended): An apparatus for automatically compensating a routing tag for a cell based on an address provided by a bus operation on a bus connected to a first node of a system for network computing;

an address capturing mechanism configured to capture said address from said bus;

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an address compensation mechanism configured to convert said address from said bus into a value stored in said routing tag of said cell;

a first cell generation mechanism at said first node configured to convert said bus operation into said cell;

a first cell transportation mechanism configured to transport said cell over said system interconnect from said first node to a second node; and

a bus operation mechanism at said second node configured to perform an equivalent bus operation on a second computer system bus after receipt of said cell by said second node.

150. (Previously Presented): The apparatus of claim 141 wherein the first cell generation mechanism further comprises:

an address mapping circuit addressable memory (AMCAM) responsive to said bus operation to determine an identifier for said first node; and

a cell address translation configured to include said identifier in said cell.

151. (Previously Presented): The apparatus of claim 141 wherein said first bus is a first PCI bus and said second bus is a second PCI bus.

152. (Previously Presented): The apparatus of claim 141 wherein said first bus is a PCI bus and said second bus is a bus.

151. (Continued) The apparatus of claim 149 further comprising:

a result acquisition mechanism at said second node configured to obtain a result from performance of said equivalent bus operation on said second bus;

a second cell generation mechanism at said second node configured to convert said result into a second cell;

a second cell transportation mechanism at said second node configured to transmit said second cell over said system interconnect from said second node to said first node; and

a bus operation completion mechanism at said first node configured to complete said bus operation on receipt of said second cell.

154. (Continued).

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